REMARKS

In the Office Action[1], the Examiner took the following actions:

> rejected claims 2, 4-9, 13-15, and 21-24 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Publication No. 2002/0190375 A1 (that matured to U.S. Patent No. 6,699,787, on March 2, 2004, "Mashino") in view of U.S. Publication No. 2002/0115226 A1 (that matured to U.S. Patent No. 6,963,095, on November 8, 2005, "Mikawa");
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> rejected claims 10-12 under 35 U.S.C. § 103(a) as being unpatentable over Mashino, Mikawa, and U.S. Publication No. 2001/0045605 A1 (that matured to U.S. Patent No. 6,869,867, on March 22, 2005, "Mayashita"); and
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> rejected claims 16-20 under 35 U.S.C. § 103(a) as being unpatentable over Mashino, Mikawa, and U.S. Patent No. 6,166,425 ("Sakao").

Applicant has amended claims 2, 7, 9, and 20. For example, claim 2 has been amended to recite "a through plug formed to have a side surface being in contact with the diffusion layer patterns, the side surface surrounded by the diffusion layer patterns without being in contact with the insulation film, and to pass through the diffusion layer patterns and the semiconductor substrate," to even more clearly define the claimed "through plug." Claims 7, 9, and 20 are also amended to even more clearly the define the "through plug[s]" recited respectively therein. Support for the amendments to claims 2, 7, 9, and 20, can be found, for example, in Fig. 1B of Applicant's specification.

[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicant declines to automatically subscribe to any statement or characterization in the Office Action.

Applicant respectfully traverses the rejection of claims 2, 4-9, 13-15, and 21-24 under 35 U.S.C. § 103(a) as being unpatentable over Mashino in view of Mikawa. No *prima facie* case of obviousness can be established based on these references.

To establish a *prima facie* case of obviousness, three basic criteria must be satisfied. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine references. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all of the claim elements. *See* M.P.E.P. § 2143. Moreover, the requisite teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in Applicant's disclosure. *See In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). *See* M.P.E.P. § 706.02(j). No *prima facie* case of obviousness can be established because the combination of Mashino and Mikawa fails to teach each and every element of the claimed "through plug" recited in claim 2.

Claim 2 recites "a through plug formed to have a side surface being in contact with the diffusion layer patterns, the side surface being surrounded by the diffusion layer patterns without being in contact with the insulation film, and to pass through the diffusion layer patterns and the semiconductor substrate."

Mashino teaches a through hole 212 filled with conductor 217 (paragraph [0146]). The Examiner concedes that Mashino fails to teach a "semiconductor element

formation layer . . . [including] diffusion layer patterns" (Office Action at 4), but contends that Mashino's semiconductor element formation layer 202 requires diffusion layer patterns, as taught by Mikawa (Office Action at 2-3).

Even assuming that the Examiner's conclusions are correct, and Applicant does not agree that they are, Mashino does not disclose that conductor 217 is in contact with element formation layer 202. Mashino, Fig. 10. Instead, the reference teaches that conductor 217, to the extent that it corresponds to the claimed "through plug," is formed in contact with interconnect pattern 214. Id.

Thus, Mashino does not teach a "through plug" formed "hav[ing] a side surface being in contact with the diffusion layer patterns." Accordingly, Mashino fails to teach "a through plug formed to have a side surface being in contact with the diffusion layer patterns, the side surface being surrounded by the diffusion layer patterns without being in contact with the insulation film, and to pass through the diffusion layer patterns and the semiconductor substrate," as recited in claim 2.

Mikawa also fails to teach the claimed "through plug," as recited in claim 2. Mikawa teaches contact plug 14 is formed within intermediate isolation film 13 between lower electrode 15 and heavily doped diffusion layers 11a. Mikawa, Fig. 1. Mikawa, however, fails to teach "a through plug formed to have a side surface being in contact with the diffusion layer patterns, the side surface being surrounded by the diffusion layer patterns without being in contact with the insulation film, and to pass through the diffusion layer patterns and the semiconductor substrate," as recited in claim 2 (emphasis added).

No *prima facie* case of obviousness can therefore be established based on Mashino and Mikawa with respect to claim 2 because the cited references, either alone or in combination, fail to teach or suggest the claimed "through plug . . . ."

Claim 7 recites "a through plug formed to have a side surface being in contact with the insulation film, the side surface being surrounded by the insulation film without being in contact with the diffusion layer patterns, and to pass through the insulation film and the semiconductor substrate, the through plug being partly surrounded by the pattern portion above the diffusion layer patterns and/or the insulation film and being insulated from the pattern portion."

The Examiner concedes that Mashino fails to teach a "semiconductor element formation layer . . . [including] an insulating layer formed between the plural diffusion layer patterns on the semiconductor substrate" (Office Action at 6). As discussed above Mashino teaches that conductor 217 is formed in contact with interconnect pattern 214 but fails to teach or suggest that conductor 217 is formed in contact with formation layer 202, to the extent that these elements even correspond to the claimed "through plug" and "insulation film," respectively. Accordingly, Mashino does not teach "a through plug formed to have a side surface being in contact with the insulation film," as recited in claim 7.

Mikawa teaches that isolation films 12 are formed in between diffusion layers 11a and that contact plug 14 is formed in contact with diffusion layers 11a. Mikawa, Fig. 1. Mikawa, however, fails to teach or suggest "a through plug formed to have a side surface being in contact with the insulation film [formed between the diffusion layer

patterns on the semiconductor substrate to isolate the diffusion layer patterns from one another]," as recited in claim 7 (emphasis added).

No *prima facie* case of obviousness can thus be established based on the combination of Mashino and Mikawa with respect to claim 7 because the references, either alone or in combination, fail to teach "a through plug formed to have a side surface being in contact with the insulation film," (emphasis added) as recited in claim 7.

Claim 9, although of different scope, recites similar elements as claims 2 and 7. No *prima facie* case of obviousness can be established with respect to claim 9 for the above discussed reasons based on the combination of Mashino and Mikawa. Moreover, claims 4-6, 8, 13-15, and 21-24 depend from independent claims 2, 7 and 9 and are allowable at least due to their dependence. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 2, 4-9, 13-15, and 21-24 based on Mashino and Mikawa.

Applicant respectfully traverses the rejection of claims 10-12 under 35 U.S.C. §103(a) as being unpatentable over Mashino, Mikawa, and Mayashita. Claims 10-12 depend from independent claims 7, 2, and 9, respectively, and thus require each and every element recited in each of their respective independent claims. As set forth above, claims 7, 2, and 9, recite elements not taught by Mashino and Mikawa. Mayashita discloses a "semiconductor device of a MIS" structure (paragraph [0001]), but also fails to teach or suggest the claimed "through plug" recited in claims 7, 2, and 9, and required by claims 10-12. Accordingly, no *prima facie* case of obviousness can be established with respect to claims 10-12. Applicant respectfully requests the Examiner reconsider and allow claims 10-12.

Applicant respectfully traverses the rejection of claims 16-20 under 35 U.S.C. § 103(a) as being unpatentable over Mashino, Mikawa, and Sakao. Claims 16-20 depend from corresponding independent claims 2, 7, or 9. As set forth above, claims 2, 7, and 9 recite elements not taught by Mashino and Mikawa. Sakao also fails to teach these elements. Sakao is drawn to a "semiconductor device including a MOS transistor and a resistance element with a large resistivity." However, Sakao also fails to teach or suggest the claimed "through plug" recited in independent claims 2, 7, and 9, and required by their corresponding dependent claims 16-20. Accordingly, no *prima facie* case of obviousness can be established with respect to claims 16-20. Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 16-20.

In view of the foregoing amendments and remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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